1. An address translation filter for filtering a signal on a system bus comprising:

a first interface operable to connect to the system bus and receive a virtual memory address;

a second interface operable to connect to the system bus and transmit a physical memory address; and

an address translation unit operable to determine the physical memory address from the virtual memory address.

2. An address translation filter in accordance with claim 1, wherein the address translation unit includes a lookup table indexed by virtual addresses.

3. An address translation filter in accordance with claim 2, wherein the lookup table is indexed by the most significant portion of a virtual address.

4. An address translation filter in accordance with claim 1, wherein the address translation unit comprises a translation lookaside buffer.

5. An address translation filter in accordance with claim 4, further comprising:

a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation

lookaside buffer.

6. An address translation filter in accordance with claim 5, further comprising:

an output control link responsive to the refresh logic unit and operable to signal a core processor when the translation lookaside buffer is to be refreshed.

7. An address translation filter in accordance with claim 5, further comprising:

an input for receiving an input system clock signal; and

an output for transmitting an output system clock signal,

wherein the output clock signal is paused while the translation lookaside buffer is being refreshed.

8. An address translation filter in accordance with claim 1, wherein the virtual and physical memory addresses have the same width.

9. A digital processing system, comprising:

a core processor;

an external memory unit;

an external processing device;

an address translation filter; and

a system bus linking the core processor, the external memory and the address translation filter to each other and linking the external processing device to the address translation filter,

wherein the address translation unit is operable to translate a virtual memory address received via the system bus from the external processing device into a physical memory address transmitted via the system bus to the external memory unit.

10. A digital processing system in accordance with claim 9, wherein the address translation filter comprises:

a translation lookaside buffer; and

a refresh logic unit operable to refresh the translation lookaside buffer when the virtual memory address is not matched by an entry in the translation lookaside buffer.

11. A digital processing system in accordance with claim 10, wherein the address translation filter further comprises:

an output control link responsive to the refresh logic unit and operable to send a refresh signal the core processor when the translation lookaside buffer is to be refreshed.

12. A digital processing system in accordance with claim 10, wherein the core processor is operable to refresh the translation lookaside buffer when a refresh signal is received from the address translation filter.

13. A digital processing system in accordance with claim 12, wherein the translation lookaside buffer is refreshed via the system bus.

14. A digital processing system in accordance with claim 9, wherein the bus is one of an AMBA bus and an AHB bus.

15. A method of memory address translation comprising:

receiving a first bus signal;

translating a virtual memory address specified by the first bus signal to a physical memory address in an address translation filter; and

transmitting a second bus signal in accordance with the physical memory address.

16. A method in accordance with claim 15, wherein the translating comprises:

selecting a physical memory address from a table of physical memory addresses, the table of physical memory addresses being indexed by virtual addresses.

17. A method in accordance with claim 16, further comprising:

refreshing the table of physical memory addresses if the table has no entry for the virtual address.

18. A method in accordance with claim 17, wherein the refreshing comprises receiving data via the bus from a core processor coupled to the bus.

19. A method in accordance with claim 17, wherein the refreshing comprises:

signaling a core processor that the table of physical memory addresses needs to refreshed;

passing the virtual memory address to the core processor; and

receiving a new physical memory address from the core processor.

20. A method in accordance with claim 17, wherein the first bus signal is received from a processing device, further comprising:

providing a system clock signal to the processing device; and

pausing the system clock signal while the table of physical memory addresses is being refreshed.

21. A method in accordance with claim 15, wherein the second bus signal is transmitted to an external memory unit.

22. A method in accordance with claim 15, wherein the first bus signal is received from a processing device.

23. A method in accordance with claim 22, further comprising:

transferring code from a core processor to the processing device; and

transferring an initial memory map from the core processor to the address translation filter.